```
=> d his

     (FILE 'USPAT' ENTERED AT 08:58:01 ON 06 JUL 1998)
L1          7673 S (LOAD? (3A) BUFFER#)
L2           195 S L1/AB
L3             1 S L2 (P) (NON BLOCK?)
L4          9040 S (LIMIT? (3A) (ADMISSION# OR ACCESS?))
L5           215 S L1 AND L4
L6            15 S L1 (P) L4
L7          1531 S L4 (P) (TRANSACTION# OR TASK# OR PROCESS?)
L8            38 S L7 (P) PRIORIT?
L9          1645 S (PRIORIT? (3A) (BUFFER# OR QUEUE# OR FIFO#))
L10          173 S L9 (7A) (PLURALITY OR MULTIPLE OR DIFFERENT OR SEVERAL)
L11           55 S L10/AB,CLM
L12            6 S L4 AND L10
L13           83 S L7 AND L9
L14            3 S L7 (P) L9
L15        16016 S (CHANNEL? (3A) (TRANSACTION# OR TASK# OR PROCESS?))
L16           27 S L10 AND L15
L17            3 S L10 (P) L15

     FILE 'JPOABS' ENTERED AT 09:54:00 ON 06 JUL 1998
L18            4 S L10
L19           63 S L7
L20            2 S L8
L21         1935 S L15
L22            1 S L19 AND L21

     FILE 'EPOABS' ENTERED AT 09:58:58 ON 06 JUL 1998
L23           74 S L7
L24            5 S L8
L25           11 S L10
L26         1280 S L15
```

=> d l18 3 all

62-98841 May 8, 1987 L18: 3 of 4

INTERRUPTION PACKET TRANSMISSION SYSTEM

INVENTOR: YOSHITAKA HIRANO, et al. (2)
ASSIGNEE: NIPPON TELEGR & TELEPH CORP <NTT>
APPL NO: 60-236450
DATE FILED: Oct. 24, 1985
PATENT ABSTRACTS OF JAPAN
ABS GRP NO: E546
ABS VOL NO: Vol. 11, No. 306
ABS PUB DATE: Oct. 6, 1987
INT-CL: H04L 11/20; H04J 3/16

ABSTRACT:

PURPOSE:To reduce the delay of a transmitting packet with a higher emergency by prioritizing each packet, installing an interruption inhibiting area on the back of the packet, and abandoning the packet under transmission so as to interruptingly transmit the highly prioritized packet if a request transmitting the packet with the higher priority than that of the packet under transmission is issued.

CONSTITUTION:A priority decision processing part 32 prioritizes reception packets 1.approx.n and transmits them to **queues** with **different priorities**. A transmission order control part 35 transmits a transmission permitting signal ACKi to the queue Qi with the top priority among said queues with an ON transmission request signal. If the queue Qj with the higher priority than that of the packet Pi currently transmitted requests transmission in the middle of transmissing the packet Pi, the transmission order control part 35 transmits an interruption request signal INTREQ=ON to an interruption processing part 36. Receiving the INTACK=ON, the transmission order control part 35 makes the ACKi equal to OFF. Simultaneously a transmission processing part 34 stops the transmission of the packet Pi, turns ON the transmission permitting signal ACKj with respect to the top priority queue Qj, and starts transmitting the top priority packet Pj.

US PAT NO: 4,271,468 [IMAGE AVAILABLE] L17: 2 of 3
TITLE: Multiprocessor mechanism for handling channel interrupts

SUMMARY:

BSUM(19)

The . . . invention provides an improved system allowing simultaneous control of a plurality of central processors (CPs) for selecting the CPs to **process** pending **channel** interrupts (CIs) on a plurality of CI queues in main storage. A **channel processor** receives interrupt signals from a plurality of I/O control units, I/O devices, their subchannels and the channel. For each pending interrupt signal it receives, the **channel processor** posts an interrupt request (IR) entry to one of the queues it selects in accordance with a preassignment of queues to the source and type of interrupt. The **channel processor** only puts entries on the CI queues but does not process or remove entries from the queues. Queue entries are only removed and processed by selected central processors (CPs) in the multiprocessor system. The CI **queues** are assigned **different priorities** in accordance with the speed required for processing the interrupts pending on them. On any single queue, the entries are. . .

SUMMARY:

BSUM(21)

An interrupt queue pending (PND) register is provided in the CI controller which has register positions respectively assigned to the **different** CI **queues** in their **priority** sequence. The set/reset state of the corresponding positions in the pending register indicate the non-empty/empty condition of the respective CI queues in main storage. Each time the **channel processor** sends an interrupt command, the CI controller sets the corresponding queue position in the pending register to indicate a non-empty. . .

US PAT NO: 4,837,688 [IMAGE AVAILABLE] L17: 1 of 3
TITLE: Multi-channel shared resource processor

DETDESC:

DETD(2)

Referring . . . 10 described herein includes a plurality of task queues 12, a dispatcher system 14, an execution unit such as a multi-**channel** shared resource **processor** (MSRP) 16 and memory system 18. The MSRP 16 includes eight distinct **processor channels** P0 through P7, which utilize the memory system 18 and a central processing unit (CPU) 20. The dispatcher 14 distributes tasks appearing in task **queues** 12 having **different priorities** to the **processor channels** P0 through P7. The MSRP 16 switches between the **processing channels** during an instruction cycle in order to service the tasks having the highest priorities. The MSRP 16 further includes eight program counters which are associated with the eight **processor channels** P0 through P7. Each of the **processor channels** uses its respective program counter to maintain an instruction stream. This architecture eliminates the need to interrupt an instruction stream in a single **processor channel** working on a first task for a context switch to a second task. The instruction cycle starts by reading an encoded instruction from the memory system 18, executing the instruction and ends by storing information in the **processor channel**'s exclusive section of the memory system 18 and the **processor channel**'s exclusive working registers in the CPU 20. Thus, each instruction cycle ends without storing any residual information in the CPU 20 resources that are shared amoung the eight **processor channels** P0 through P7 which then facilitates an instantaneous change to another **processor channel**'s instruction s

US PAT NO: 5,752,193 [IMAGE AVAILABLE] L14: 1 of 3
TITLE: Method and apparatus for communicating in a wireless communication system

DETDESC:

DETD(13)

In order to facilitate transfer of higher priority data, preferably two procedures are employed to **limit** MS **access** requests. The first is the broadcasting of a current service priority message. This message communicates a minimum QOS grade/priority for. . . prevent more than peak loading of the access and/or traffic channels. Each MS having data to transfer determines in its **processor** the priority level of the data message, and inhibits any access request if the priority level is less than the. . . data priority (and billing) level to a level high enough to permit access requests. Additionally, if other packets of higher **priority** are **queued** in the MS, the MS may chose to transmit the higher priority data packets ahead of a currently **queued** lower **priority** packet.

US PAT NO: 5,742,592 [IMAGE AVAILABLE] L14: 2 of 3
TITLE: Method for communicating data in a wireless communication system

DETDESC:

DETD(13)

In order to facilitate transfer of higher priority data, preferably two procedures are employed to **limit** MS **access** requests. The first is the broadcasting of a current service priority message. This message communicates a minimum QOS grade/priority for. . . prevent more than peak loading of the access and/or traffic channels. Each MS having data to transfer determines in its **processor** the priority level of the data message, and inhibits any access request if the priority level is less than the. . . data priority (and billing) level to a level high enough to permit access requests. Additionally, if other packets of higher **priority** are **queued** in the MS, the MS may chose to transmit the higher priority data packets ahead of a currently **queued** lower **priority** packet.

US PAT NO: 5,381,413 [IMAGE AVAILABLE] L14: 3 of 3
TITLE: Data throttling system for a communications network

CLAIMS:

CLMS(1)

We . . .
memory and said media access controller, and separate from said media access controller, for maintaining one or more protocols for **processing** said first and second types of data packets, for determining priority of the data packets and for executing a throttling algorithm for controlling the submission of data packets based on said determined **priority** from said **queues** to said media access controller depending on the type of data packets, to provide an

appropriate amount of bandwidth to, and to **limit** an **access** delay of said first [redacted]e of data packets in said shar[redacted] transmission medium.

CLAIMS:

CLMS(2)

2. . . . of data packets having different priorities, comprising:
at least: one protocol stack containing a plurality of protocols including one for **processing** each of said first and said other types of data packets,
a plurality of queues including a queue for each protocol. . . . access controller, which is unable to differentiate among said first type and said other types of data packets having different **priorities** stored in said **queues** to access said transmission medium with arbitrary priority, and
a throttler, separate from said media access controller, for ascertaining priority of. . . on said ascertained priority and the types of data packets, to provide an appropriate amount of bandwidth to and to **limit** an **access** delay of said first type of data packets in said shared transmission medium.

=> d 1-6 ti,kwic

US PAT NO: 5,758,184 [IMAGE AVAILABLE] L12: 1 of 6
TITLE: System for performing asynchronous file operations requested by runnable threads by processing completion messages with different queue thread and checking for completion by runnable threads

DETDESC:

DETD(13)

The . . . and applications/clients (e.g. application programs 50 and Win32 clients 52) run, with a limited set of interfaces available and with **limited access** to system data.

DETDESC:

DETD(29)

The Windows NT kernel supports 31 **different priorities**. There is a **queue** for each of the 31 priorities that contains all the ready threads at that priority. When a CPU becomes available, . . .

US PAT NO: 5,598,575 [IMAGE AVAILABLE] L12: 2 of 6
TITLE: Multiprocessor data memory sharing system in which access to the data memory is determined by the control processor's access to the program memory

SUMMARY:

BSUM(15)

While . . . be time-shared between alternate DMA and computer accesses such that neither experiences delay. On the other hand, if speed is **limited** by the memory **access** time, then prior art techniques require that one process or the other, either computation or I/O, be put on hold. . .

DETDESC:

DETD(6)

The . . . come, first served basis. The DMA controller can furthermore comprise means to form plural queues of access requests of like **priority**, the **different queues** having **different priorities**. A lower **priority queue** receives access grants only when all higher priority queues are empty. Alternatively, separate, linear queues of equal priority can be. . .

US PAT NO: 5,448,698 [IMAGE AVAILABLE] L12: 3 of 6
TITLE: Inter-processor communication system in which messages are stored at locations specified by the sender

DETDESC:

DETD(18)

While . . . work queue that is stored in the interconnect interface, it will be apparent to those skilled in the art that **multiple** work **queues** having **different priorities** may be used. In addition, the actual work queues may be located in the host memory. In this case, pointers. . .

DETDESC:

DETD(26)

Having . . . and write the various registers via load and store operations, respectively. The memory mapping table also provides a means for **limiting access** to the various registers. By assigning the registers to addresses that are only accessible to the operating system, the ability. . .

US PAT NO: 5,381,413 [IMAGE AVAILABLE] L12: 4 of 6
TITLE: Data throttling system for a communications network

ABSTRACT:
A . . . access controller, depending on the type of the data packets, to provide an appropriate amount of bandwidth in, and to **limit** the **access** delay of, a particular type of data packets in the shared transmission medium.

SUMMARY:

BSUM(3)

1. U.S. patent application Ser. No. 07/903,855, entitled "A Process for Fair and Prioritized **Access** to **Limited** Output Buffers in a Multiport Switch," filed for Fouad A. Tobagi, Joseph M. Gang, Jr. and Allen B. Goodrich on. . .

SUMMARY:

BSUM(33)

These . . . to the MAC, depending on the type of the packets, to provide an appropriate amount of bandwidth to, and to **limit** the **access** delay of, one or more particular types of data packets in the shared transmission medium.

CLAIMS:

CLMS(1)

We . . .
media access controller depending on the type of data packets, to provide an appropriate amount of bandwidth to, and to **limit** an **access** delay of said first type of data packets in said shared transmission medium.

CLAIMS:

CLMS(2)

2. . . .
media access controller, which is unable to differentiate among said first type and said other types of data packets having **different priorities** stored in said **queues** to access said transmission medium with arbitrary priority, and
a throttler, separate from said media access controller, for ascertaining priority of. . . on said ascertained priority and the types of data packets, to provide an appropriate amount of bandwidth to

and to **limit** an **access** delay of said first type of data packets in said shared transmission medium.

CLAIMS:

CLMS(19)

19. . . .
on said determined priority and the types of data packets, to provide an appropriate amount of bandwidth to and to **limit** an **access** delay of said first type of data packets in said shared transmission medium.

CLAIMS:

CLMS(21)

21. . . .
first media access controller to said second media access controller, to provide an appropriate amount of bandwidth to and to **limit** an **access** delay of particular types of data packets in said shared transmission medium.

CLAIMS:

CLMS(36)

36. . . .
on said determined priority and the type of data packets, to provide an appropriate amount of bandwidth in and to **limit** an **access** delay of one or more types of data packets in said shared transmission medium.

CLAIMS:

CLMS(37)

37. . . .
controller depending on said determined priority and the type of packet to provide an amount of bandwidth in and to **limit** an **access** delay of one or more types of data packets in said shared transmission medium.

US PAT NO: 5,347,511 [IMAGE AVAILABLE] L12: 5 of 6
TITLE: Traffic management in packet communications networks

DETDESC:

DETD(9)

Each . . . be equipped with its own set of priority buffers 30-32, or a mechanism can be provided to enter packets from **different** sources into a common set of **priority** classification **buffers** 30-32. It should also be noted that one or more of the transmission links 34 can be connected to yet. . .

DETDESC:

DETD(59)
where .sigma..sub.i.sup.2 =m.sub.i (R.sub.i -M.sub.i) and c.sub.i.sup.(k) is computed from equation (2), assuming **different buffer** characteristics for each **priority** class, i.e., **different** values for .chi..sup.(k) and .epsilon..sup.(k) for each class k as shown in FIG. 3. The generalized link metric of equation. . .

DETDESC:

DETD(79)

As . . . prevent such congestion, a stratagem such as the leaky bucket stratagem described in the above-noted prior application is used to **limit** the **access** of that signal source to the network while the signal source is outside of the assumed statistical values. Such parameters. . .

US PAT NO: 5,305,389 [IMAGE AVAILABLE] L12: 6 of 6
TITLE: Predictive cache system

DETDESC:

DETD(12)

In . . . the system is not encountering any new information or changes in access pattern, or because it has exceeded user-specified resource **limits**. The **access** pattern information for a single access context is known as a pattern memory. The system stores each pattern memory between. . .

DETDESC:

DETD(14)

With . . . UIDs are entered in the prefetch queue 34 for processing by the server 20. Though the UIDs in the demand **queue** 32 are given **priority**, the server may look to **different** devices for the different objects, so the prefetched objects may actually be accessed in parallel with the demand objects.

=> d 1-38 ti

US PAT NO: 5,761,521 [IMAGE AVAILABLE] L8: 1 of 38
TITLE: Processor for character strings of variable length

US PAT NO: 5,752,193 [IMAGE AVAILABLE] L8: 2 of 38
TITLE: Method and apparatus for communicating in a wireless communication system

US PAT NO: 5,742,592 [IMAGE AVAILABLE] L8: 3 of 38
TITLE: Method for communicating data in a wireless communication system

US PAT NO: 5,724,599 [IMAGE AVAILABLE] L8: 4 of 38
TITLE: Message passing and blast interrupt from processor

US PAT NO: 5,689,657 [IMAGE AVAILABLE] L8: 5 of 38
TITLE: Apparatus and methods for bus arbitration in a multimaster system

US PAT NO: 5,678,007 [IMAGE AVAILABLE] L8: 6 of 38
TITLE: Method and apparatus for supporting multiple outstanding network requests on a single connection

US PAT NO: 5,651,127 [IMAGE AVAILABLE] L8: 7 of 38
TITLE: Guided transfers with variable stepping

US PAT NO: 5,642,488 [IMAGE AVAILABLE] L8: 8 of 38
TITLE: Method and apparatus for a host computer to stage a plurality of terminal addresses

US PAT NO: 5,560,030 [IMAGE AVAILABLE] L8: 9 of 38
TITLE: Transfer processor with transparency

US PAT NO: 5,551,062 [IMAGE AVAILABLE] L8: 10 of 38
TITLE: Method for enhancing communication access in a radio communication system

US PAT NO: 5,528,513 [IMAGE AVAILABLE] L8: 11 of 38
TITLE: Scheduling and admission control policy for a continuous media server

US PAT NO: 5,524,265 [IMAGE AVAILABLE] L8: 12 of 38
TITLE: Architecture of transfer processor

US PAT NO: 5,493,646 [IMAGE AVAILABLE] L8: 13 of 38
TITLE: Pixel block transfer with transparency

US PAT NO: 5,487,146 [IMAGE AVAILABLE] L8: 14 of 38
TITLE: Plural memory access address generation employing guide table entries forming linked list

US PAT NO: 5,469,577 [IMAGE AVAILABLE] L8: 15 of 38
TITLE: Providing alternate bus master with multiple cycles of bursting access to local bus in a dual bus system including a processor local bus and a device communications bus

US PAT NO: 5,381,413 [IMAGE AVAILABLE] L8: 16 of 38
TITLE: Data th[redacted]tling system for a communicati[redacted]s network

US PAT NO: 5,287,519 [IMAGE AVAILABLE] L8: 17 of 38
TITLE: LAN station personal computer system with controlled data access for normal and unauthorized users and method

US PAT NO: 5,276,681 [IMAGE AVAILABLE] L8: 18 of 38
TITLE: **Process** for fair and **prioritized access** to **limited** output buffers in a multi-port switch

US PAT NO: 5,237,567 [IMAGE AVAILABLE] L8: 19 of 38
TITLE: Processor communication bus

US PAT NO: 5,204,957 [IMAGE AVAILABLE] L8: 20 of 38
TITLE: Integrated circuit timer with multiple channels and dedicated service processor

US PAT NO: 5,201,053 [IMAGE AVAILABLE] L8: 21 of 38
TITLE: Dynamic polling of devices for nonsynchronous channel connection

US PAT NO: 5,197,125 [IMAGE AVAILABLE] L8: 22 of 38
TITLE: Access assignment in a DAMA communication system

US PAT NO: 5,170,266 [IMAGE AVAILABLE] L8: 23 of 38
TITLE: Multi-capability facsimile system

US PAT NO: 5,129,078 [IMAGE AVAILABLE] L8: 24 of 38
TITLE: Dedicated service processor with inter-channel communication features

US PAT NO: 5,117,498 [IMAGE AVAILABLE] L8: 25 of 38
TITLE: Processer with flexible return from subroutine

US PAT NO: 5,042,005 [IMAGE AVAILABLE] L8: 26 of 38
TITLE: Timer channel with match recognition features

US PAT NO: 4,952,367 [IMAGE AVAILABLE] L8: 27 of 38
TITLE: Timer channel for use in a multiple channel timer system

US PAT NO: 4,942,522 [IMAGE AVAILABLE] L8: 28 of 38
TITLE: Timer channel with multiple timer reference features

US PAT NO: 4,926,319 [IMAGE AVAILABLE] L8: 29 of 38
TITLE: Integrated circuit timer with multiple channels and dedicated service processor

US PAT NO: 4,653,112 [IMAGE AVAILABLE] L8: 30 of 38
TITLE: Image data management system

US PAT NO: 4,602,129 [IMAGE AVAILABLE] L8: 31 of 38
TITLE: Electronic audio communications system with versatile message delivery

US PAT NO: 4,511,969 [IMAGE AVAILABLE] L8: 32 of 38
TITLE: Control channel interface circuit

US PAT NO: 4,459,665 [IMAGE AVAILABLE] L8: 33 of 38
TITLE: Data processing system having centralized bus priority resolution

US PAT NO: 4,399,503 [IMAGE AVAILABLE] L8: 34 of 38
TITLE: Dynamic disk buffer control unit

US PAT NO: 4,300,194 [IMAGE AVAILABLE] L8: 35 of 38
TITLE: Data processing system having multiple common buses

US PAT NO: 4,271,505 [IMAGE AVAILABLE] L8: 36 of 38
TITLE: Process communication link

US PAT NO: 4,257,095 [IMAGE AVAILABLE] L8: 37 of 38
TITLE: System bus arbitration, circuitry and methodology

US PAT NO: 3,624,608 [IMAGE AVAILABLE] L8: 38 of 38
TITLE: VEHICLE SHARED-USE SYSTEM

=> d l6 1-15 ti

US PAT NO: 5,768,205 [IMAGE AVAILABLE] L6: 1 of 15
TITLE: Process of transfering streams of data to and from a random access memory device

US PAT NO: 5,684,753 [IMAGE AVAILABLE] L6: 2 of 15
TITLE: Synchronous data transfer system

US PAT NO: 5,680,370 [IMAGE AVAILABLE] L6: 3 of 15
TITLE: Synchronous DRAM device having a control data buffer

US PAT NO: 5,680,369 [IMAGE AVAILABLE] L6: 4 of 15
TITLE: Synchronous dynamic random access memory device

US PAT NO: 5,680,368 [IMAGE AVAILABLE] L6: 5 of 15
TITLE: Dram system with control data

US PAT NO: 5,680,367 [IMAGE AVAILABLE] L6: 6 of 15
TITLE: Process for controlling writing data to a DRAM array

US PAT NO: 5,680,358 [IMAGE AVAILABLE] L6: 7 of 15
TITLE: System transferring streams of data

US PAT NO: 5,636,176 [IMAGE AVAILABLE] L6: 8 of 15
TITLE: Synchronous DRAM responsive to first and second clock signals

US PAT NO: 5,587,962 [IMAGE AVAILABLE] L6: 9 of 15
TITLE: Memory circuit accommodating both serial and random access including an alternate address buffer register

US PAT NO: 5,400,288 [IMAGE AVAILABLE] L6: 10 of 15
TITLE: Semiconductor memory chip

US PAT NO: 5,144,551 [IMAGE AVAILABLE] L6: 11 of 15
TITLE: Computer memory management method utilizing segmentation and protection techniques

US PAT NO: 5,093,807 [IMAGE AVAILABLE] L6: 12 of 15
TITLE: Video frame storage system

US PAT NO: 5,005,135 [IMAGE AVAILABLE] L6: 13 of 15
TITLE: Dynamic correction of servo following errors in a computer-numerically controlled system and fixed cycle utilizing same

US PAT NO: 4,387,365 [IMAGE AVAILABLE] L6: 14 of 15
TITLE: Real time digital scan converter

US PAT NO: 4,215,400 [IMAGE AVAILABLE] L6: 15 of 15
TITLE: Disk address controller

=> d l8 11 kwic

US PAT NO: 5,528,513 [IMAGE AVAILABLE] L8: 11 of 38

DETDESC:

DETD(18)

However, the scheduling mechanism alone does not preclude the server from overcommitting its resources by having too many concurrently active **tasks**. Isochronous streams require precise guarantees of throughput, delay and limited jitter. The scheduling mechanism cannot meet the guarantees of delay and jitter for an unbounded number of isochronous streams. One mechanism to limit the delay for servicing an isochronous **task** is to provide **priority** for these **tasks** over the real-time and general purpose **tasks**. This is done in a controlled fashion but this only limits the delay suffered by isochronous streams as a result of lower **priority** real-time and general-purpose **tasks** in the system. Even for the higher **priority** isochronous **tasks**, there needs to be enough resources existing to fulfill the **processing** requirements and meet real-time guarantees. The **admission** control policy **limits** the number of active **tasks** to a feasibly

? ds

Set	Items	Description
S1	2539	(PRIORITY (3N) (QUEUE? OR BUFFER?))
S2	2156	(PRIORITY (3N) QUEUE?)
S3	232	S1 (S) STOR?
S4	232	S1 (S) STOR???
S5	153	S2 (S) STOR???
S6	5	S4 (S) (UNDERRUN OR OVERRUN OR (SPACE (2N) AVAILABL?))
S7	67	S4 (S) (HIGH OR HIGHER OR LOW OR LOWER)
S8	26	S4 (S) (HIGH OR HIGHER) (S) (LOW OR LOWER)
S9	16	S4 (7N) (HIGH OR HIGHER) (7N) (LOW OR LOWER)
S10	12	S4 (5N) (HIGH OR HIGHER) (4N) (LOW OR LOWER)
S11	109	S1 (5N) (HIGH OR HIGHER) (4N) (LOW OR LOWER)
S12	4	S1 (5N) (HIGH OR HIGHER) (4N) (LOW OR LOWER) (5N) STOR?

12/9/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5016124 INSPEC Abstract Number: C9509-6150N-057
Title: Dynamic load sharing algorithm with a weighted load representation
Author(s): Seung Ho Cho; Sang Young Han
Author Affiliation: Dept. of Comput. Eng., Kangnam Univ., South Korea
Conference Title: Proceedings of the Thirteenth Annual ACM Symposium on Principles of Distributed Computing p.385
Publisher: ACM, New York, NY, USA
Publication Date: 1994 Country of Publication: USA ix+406 pp.
ISBN: 0 89791 654 9
U.S. Copyright Clearance Center Code: 0 89791 654 9/94/0008.$3.50
Conference Title: Proceeding of 13th ACM Symposium on Principles of Distributed Computing
Conference Sponsor: ACM
Conference Date: 14-17 Aug. 1994 Conference Location: Los Angeles, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: To collect execution information of processes, a multilevel feedback queue scheduling policy is adopted as a scheduling policy of a node. Multilevel feedback queue scheduling **stores** processes using less CPU time in **high priority queues** and processes using more CPU time in **low** priority queues. As a result of this scheduling, processes are classified into different queues according to execution characteristics during their life cycles. Therefore, when load sharing is needed, it is desirable for processes in low priority queues to be selected as candidates for migration. The load representation method in previous load sharing algorithms expresses a load as queue length in CPU. This method does not reflect execution characteristics of processes by assuming that all processes impose the same load on a node. To solve inaccuracy of this load representation used in the conventional algorithms, we propose the weighted load representation method which assigns graded weights to processes based on execution characteristics of processes. (0 Refs)
Descriptors: distributed algorithms; feedback; processor scheduling; queueing theory; resource allocation
Identifiers: weighted load representation; dynamic load sharing algorithm ; execution information; processes; multilevel feedback queue scheduling policy; node; CPU time; high priority queues; high priority processes; low priority queues; life cycles; migration; queue length; graded weights
Class Codes: C6150N (Distributed systems software); C1140C (Queueing theory); C4240P (Parallel programming and algorithm theory)